Non-Synchronous PWM Boost Controller

Halogen Free

General Description

The FP5203 is a boost topology switching regulator for wide operating voltage applications. It provides built-in gate driver pin for driving the external N-MOSFET. The internal compensation network minimizes external component counts, and the non-inverting input of error amplifier connects to a 0.6V precision reference voltage. The FP5203 has internal soft start and load detection.

The FP5203 is available in the small footprint SOT23-6L package to fit in space-saving PCB layout for miscellaneous application fields.

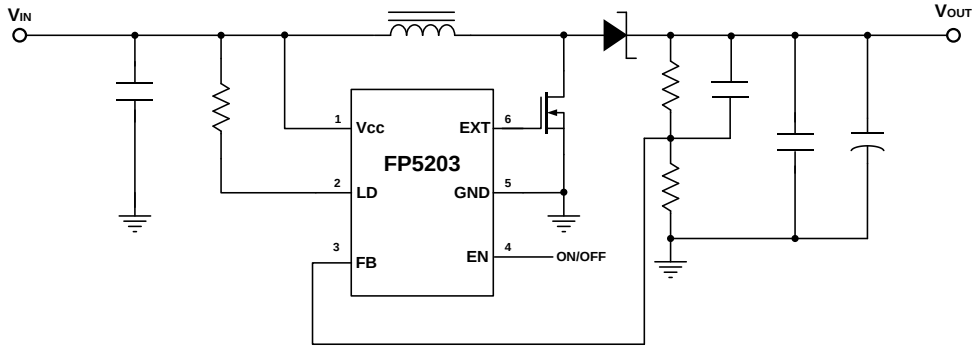
Features

- Wide Supply Voltage Operating Range: 2.4 to 5.5V
- Precision Feedback Reference Voltage: 0.6V (±2%)
- Shutdown Current: <1μA
- Internal Fixed PWM frequency: 500KHz
- Internal Soft Start Function :7ms (SS)
- Load Detection
- Over Voltage Protection
- Package: SOT23-6L
- Duty Cycle: PWM/PFM Switching Control Circuit (15%~90%)

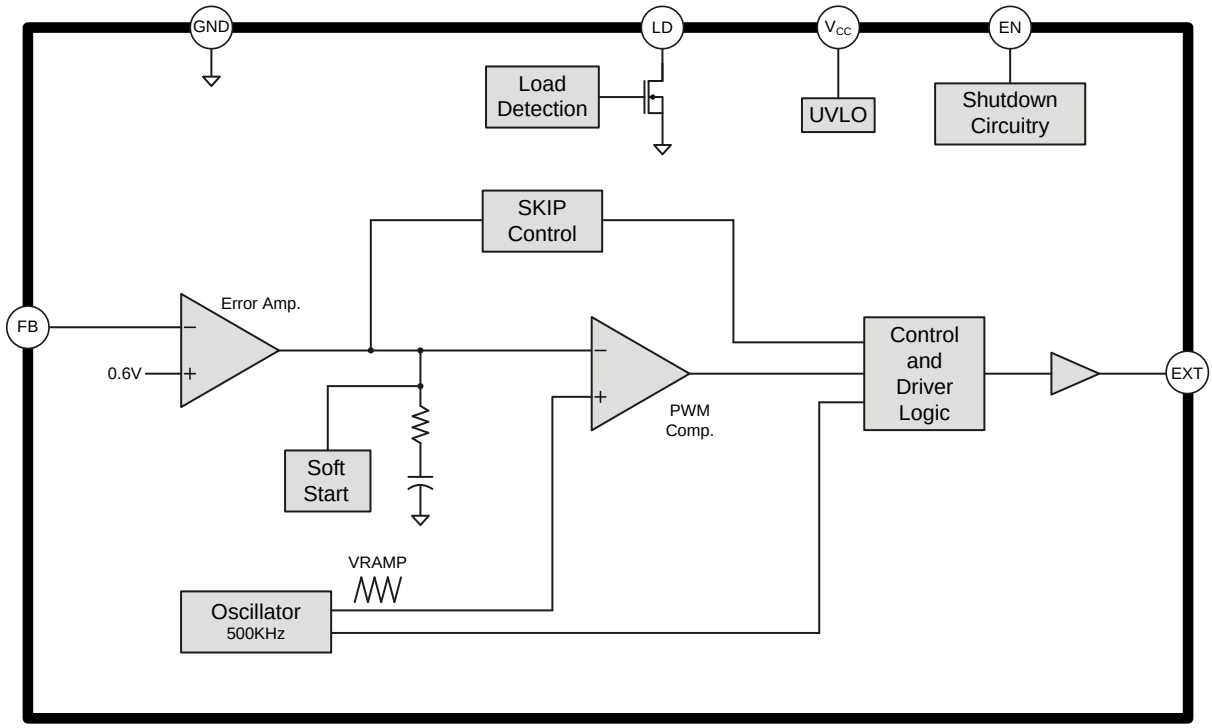
Applications

- Chargers
- LCD Displays
- Digital Cameras
- Handheld Devices
- Portable Products

Typical Application Circuit

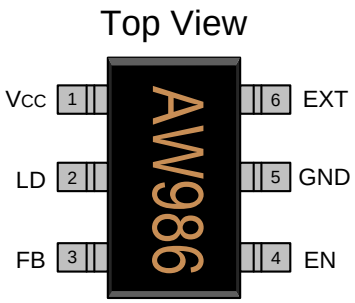


Function Block Diagram



Pin Descriptions

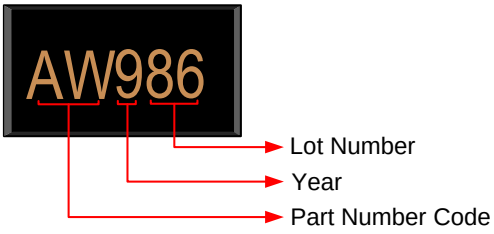
SOT23-6L



Name	No.	I / O	Description
V_{CC}	1	P	IC Power Supply
LD	2	O	Load Detection
FB	3	I	Error Amplifier Inverting Input
EN	4	I	Enable Control (Active High)
GND	5	P	IC Ground
EXT	6	O	External Transistor Connection Pin

Marking Information

SOT23-6L



Lot Number: Wafer lot number's last two digits

For Example: 132386TB → 86

Year: Production year's last digit

Part Number Code: Part number identification code for this product. It should be always "AW".

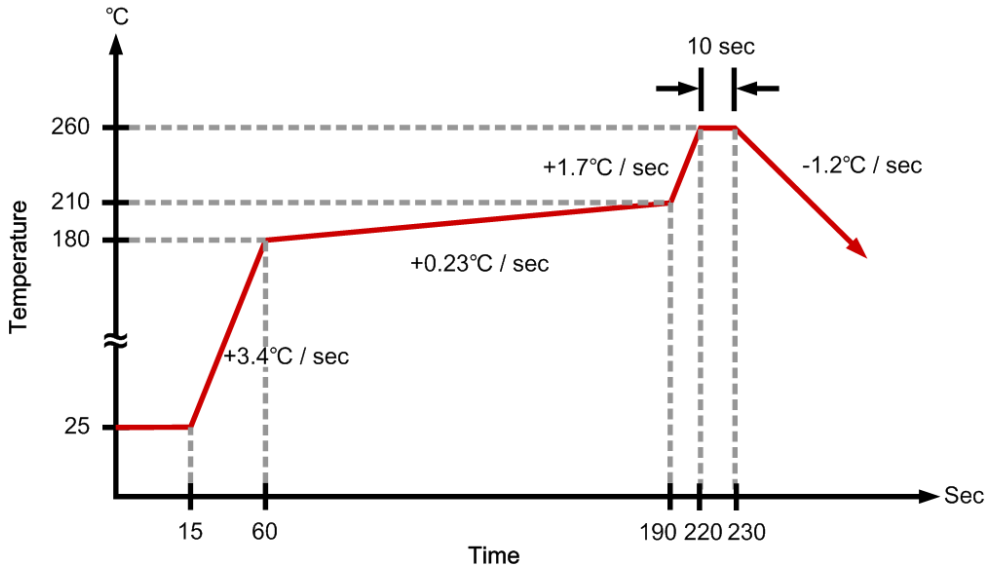
Ordering Information

Part Number	Code	Operating Temperature	Package	MOQ	Description
FP5203LR-G1	AW	-40°C ~ 85°C	SOT23-6L	3000EA	Tape & Reel

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}		0		5.5	V
EN,FB Voltage			0		5.5	V
Power Dissipation	P_D	SOT23-6L @T_A=25°C			455	mW
Thermal Resistance (Note1)	θ_{JA}	SOT23-6L			+220	°C / W
Junction Temperature	T_J				+150	°C
Operating Temperature	T_{OP}		-40		+85	°C
Storage Temperature	T_{ST}		-65		+150	°C
Lead Temperature		(soldering, 10 sec)			+260	°C

IR Re-flow Soldering Curve



Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}		2.4		5.5	V
Operating Temperature Range	T_A	Ambient Temperature	-40		+85	°C

DC Electrical Characteristics (V_{CC}=3.3V, T_A=25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
System Supply Input						
Input Supply Range	V_{CC}		2.4		5.5	V
Under Voltage Lockout	V_{UVLO}			2.1		V
UVLO Hysteresis				0.1		V
Quiescent Current	I_{CC}	FB=1.0V, No switch		70		μA
Shutdown Current	I_{CC}	V_{EN}=GND		0.1		μA
Oscillator						
Operation Frequency	f_{OSC}	V_{FB}=0.6V		500		kH_Z
PFM Switching Duty Ratio	%			15		%
Maximum Duty Ratio	%			90		%
Soft-Start Time	t_{SS}	V_{CC}=5V		7		ms
Reference Voltage						
Feedback Voltage	V_{REF}	V_{CC}=5V	0.588	0.6	0.612	V
Enable Control						
Enable Voltage	V_{EN}		0.96			V
Shutdown Voltage	V_{EN}				0.6	V
External Transistor Connection current						
EXT Pin Output Current	I_{EXTH}			-105		mA
EXT Pin Output Current	I_{EXTL}			130		mA

Function Description

Operation

The FP5203 is a voltage mode boost controller. The switching is a fixed frequency 500kHz and operates with pulse width modulation (PWM). An internal resistive divider provides 0.6V reference for the error amplifier. The FP5203 changes to PFM mode when output is light load. It can increase efficiency, but PFM mode also increases output voltage ripple.

Soft Start Function

Soft start circuitry is integrated into FP5203 to avoid inrush current during power on. After the IC is enabled, the output of error amplifier is clamped by the internal soft-start function, which causes PWM pulse width increasing slowly and thus reducing input surge current.

Shutdown Function

Drive Enable pin to ground to shut down the FP5203. Shutdown mode forces to turn off all internal circuitry, and reduces the V_{CC} supply current to 0.1μA (typ). The Enable pin rising threshold is 0.96V (typ). Before any operation begins, the voltage at Enable pin must exceed 0.96V (typ).

Load Detection

The LD pin is an open-drain output. The resistor is connected between V_{CC} and LD pin to obtain a voltage (see figure1). The LD pin is pulled to low level when output is light load.

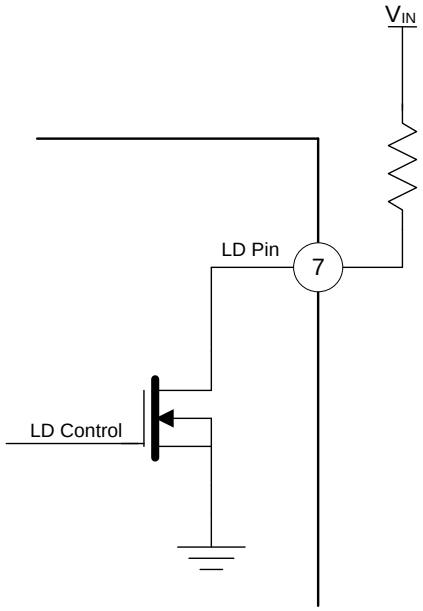


Figure1. LD pin circuit

Application Information

Inductor Selection

Inductance value is decided based on different condition. 3.3uH to 4.7μH inductor value is recommended for general application circuit. There are three important inductor specifications, DC resistance, saturation current and core loss. Low DC resistance has better power efficiency.

Capacitor Selection

The output capacitor is required to maintain the DC voltage. Low ESR capacitors are preferred to reduce the output voltage ripple. Ceramic capacitor of X5R and X7R are recommended, which have low equivalent series resistance (ESR) and wider operation temperature range.

Diode Selection

Schottky diodes with fast recovery times and low forward voltages are recommended. Ensure the diode average and peak current rating exceed the average output current and peak inductor current. In addition, the diode's reverse breakdown voltage must exceed the output voltage.

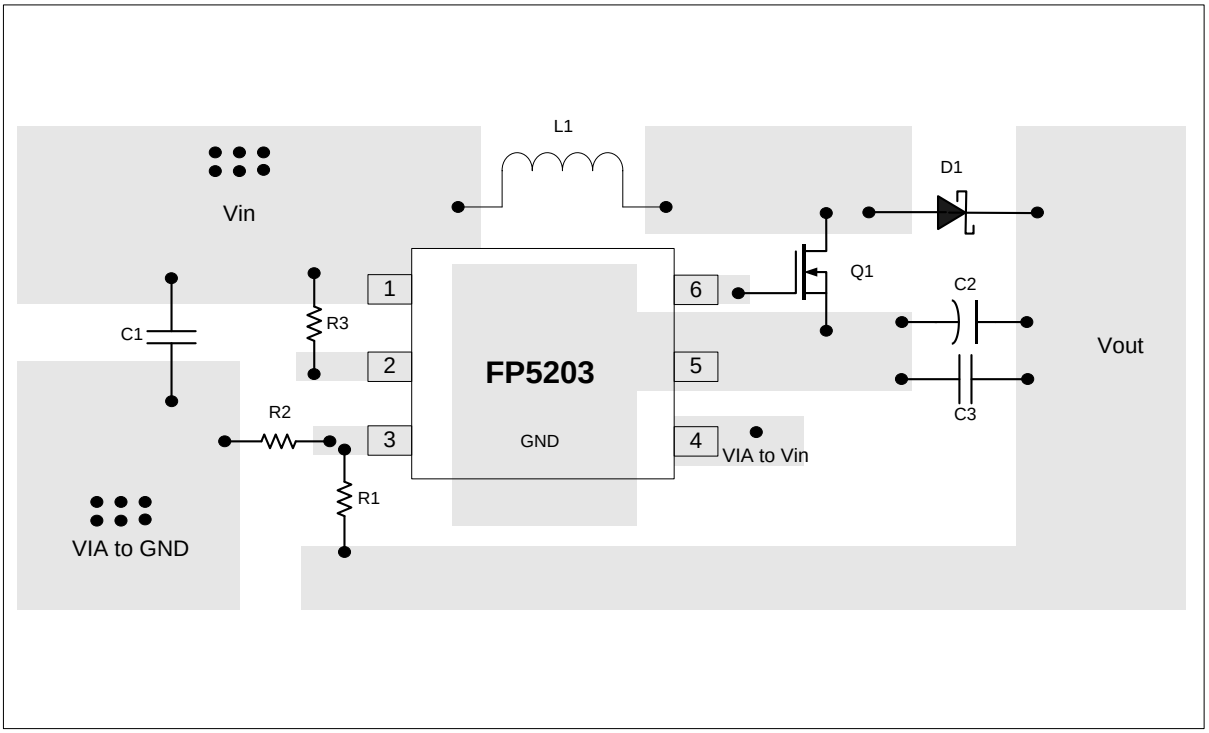
Output Voltage Programming

The output voltage is set by a resistive voltage divider from the output voltage to FB. The output voltage is:

$$V_{OUT} = 0.6V\left(1+\frac{R1}{R2}\right)$$

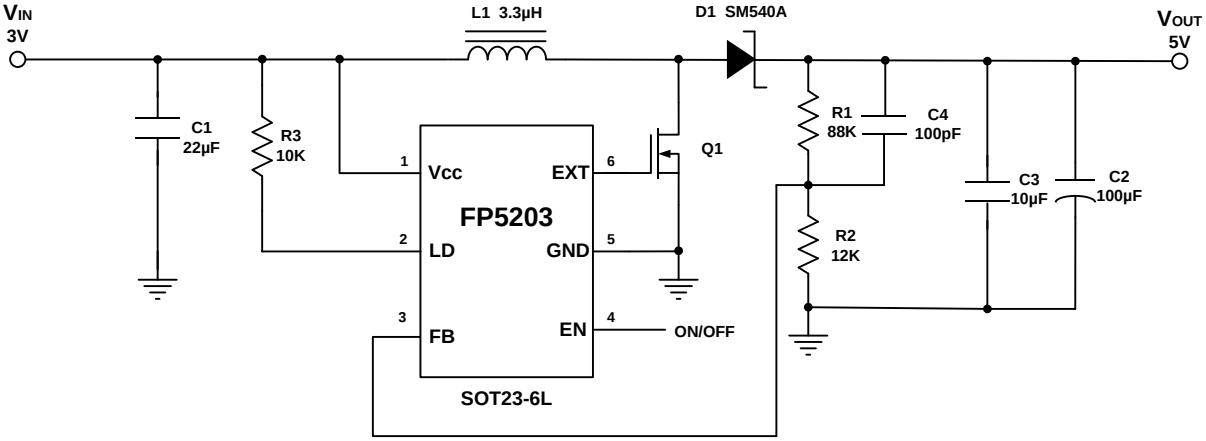
Layout Considerations

1. The power traces, consisting of the GND trace, the MOS drain trace and the V_{CC} trace should be kept short, direct and wide.
2. Layout switching node MOS drain, inductor and diode connection traces wide and short to reduce EMI.
3. Place C_{IN} near V_{CC} pin as closely as possible to maintain input voltage steady and filter out the pulsing input current.
4. The resistive divider R1and R2 must be connected to FB pin directly as closely as possible.
5. FB is a sensitive node. Please keep it away from switching node, MOS drain.
6. The GND of the IC, C_{IN} and C_{OUT} should be connected close together and directly to a ground plane.



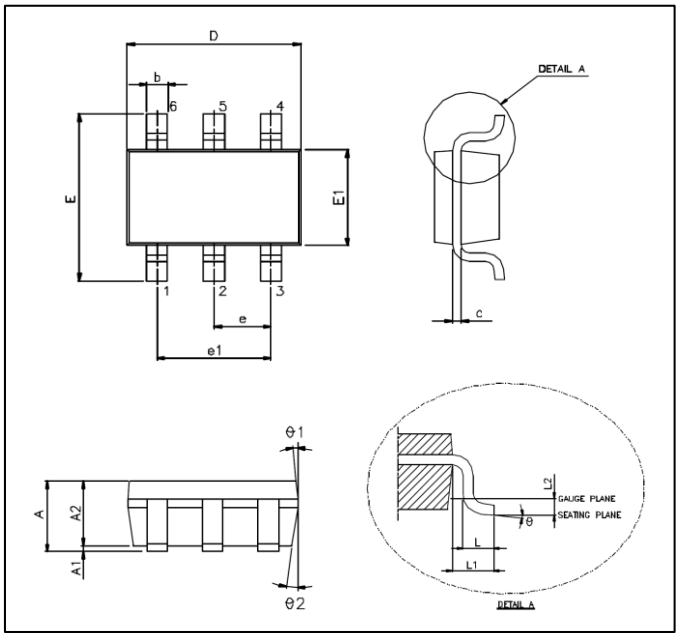
Suggested Layout

Application Information



Package Outline

SOT23-6L



Unit: mm

Symbols	Min. (mm)	Max. (mm)
A	1.050	1.450
A1	0.050	0.150
A2	0.900	1.300
b	0.300	0.500
c	0.080	0.220
D	2.900 BSC	
E	2.800 BSC	
E1	1.600 BSC	
e	0.950 BSC	
e1	1.900 BSC	
L	0.300	0.600
L1	0.600 REF	
L2	0.250 BSC	
θ°	0°	8°
θ1°	3°	7°
θ2°	6°	15°

Note:

1. Package dimensions are in compliance with JEDEC outline: MO-178 AB.
2. Dimension “D” does not include molding flash, protrusions or gate burrs.
3. Dimension “E1” does not include inter-lead flash or protrusions.