

Non-Synchronous PWM Boost Controller



General Description

The FP5209 is a boost topology switching regulator for wide operating voltage applications. It provides built-in gate driver pin, EXT pin, for driving the external N-MOSFET. The internal compensation network minimizes external component counts, and the non-inverting input of error amplifier connects to a 0.6V precision reference voltage. The FP5209 have internal soft start function.

The FP5209 is available in the small footprint SOT23-5L package to fit in space-saving PCB layout for miscellaneous application fields.

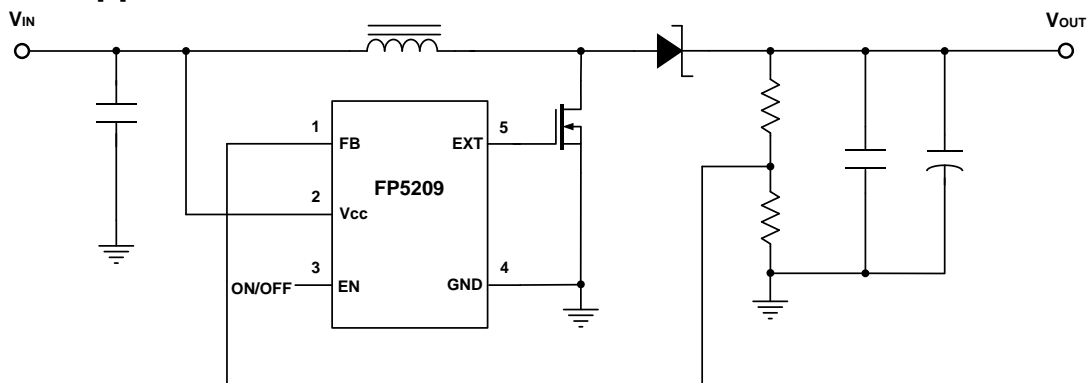
Features

- Wide Supply Voltage Operating Range: 2.4 to 5.5V
- Precision Feedback Reference Voltage: 0.6V ($\pm 2\%$)
- Shutdown Current: $< 1\mu\text{A}$
- Internal Fixed PWM frequency: 550KHz
- Internal Soft Start Function :7ms (SS)
- Over Voltage Protection
- Package: SOT23-5L
- Duty Cycle: PWM/PFM Switching Control Circuit (15%~90%)

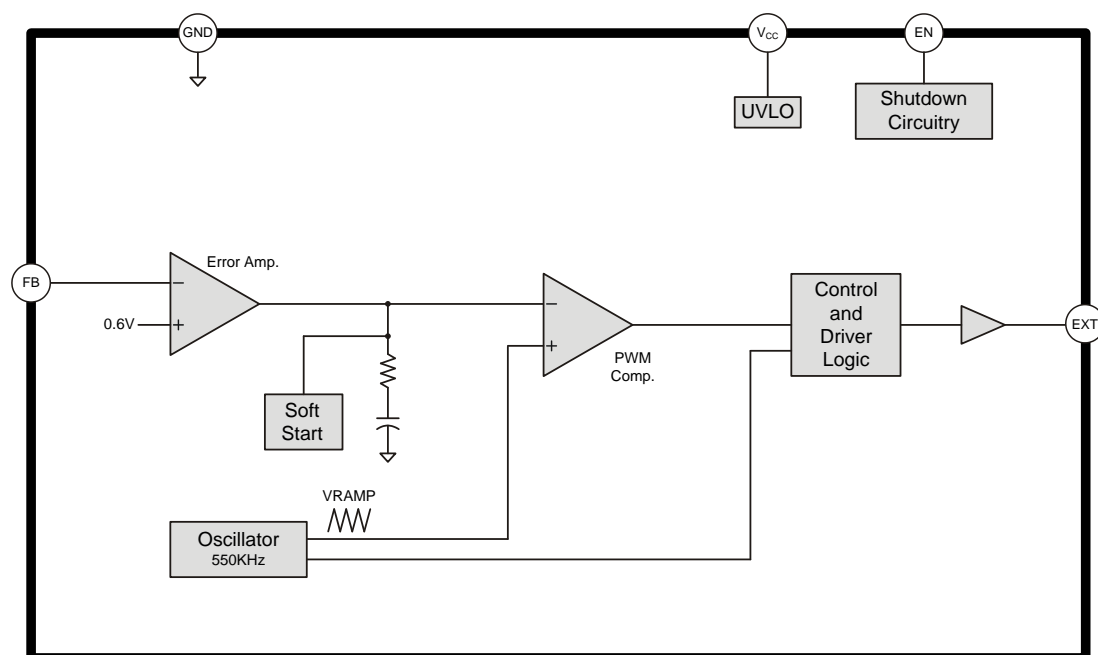
Applications

- Chargers
- LCD Displays
- Digital Cameras
- Handheld Devices
- Portable Products

Typical Application Circuit

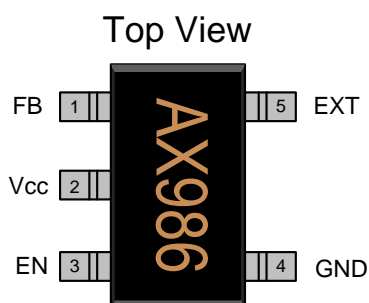


Function Block Diagram



Pin Descriptions

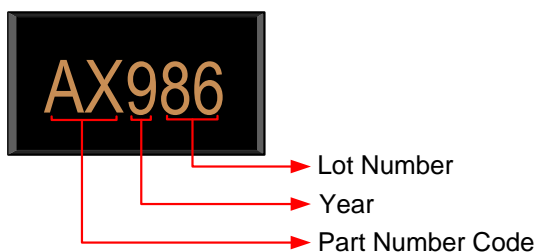
SOT23-5L



Name	No.	I / O	Description
FB	1	I	Error Amplifier Inverting Input
Vcc	2	P	IC Power Supply
EN	3	I	Enable Control (Active High)
GND	4	P	IC Ground
EXT	5	O	External Transistor Connection Pin

Marking Information

SOT23-5L



Lot Number: Wafer lot number's last two digits

For Example: 132386TB → 86

Year: Production year's last digit

Part Number Code: Part number identification code for this product. It should be always "AX".

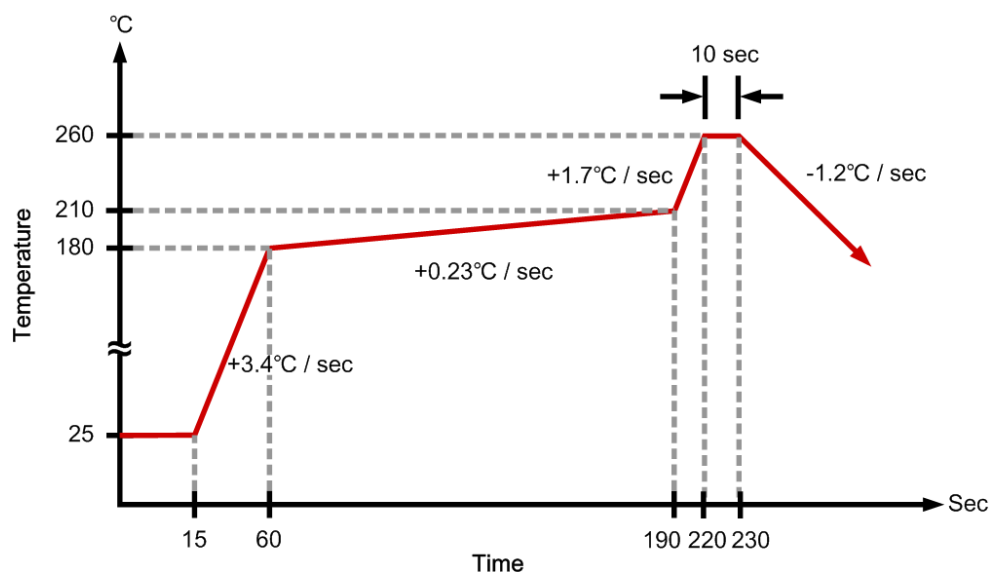
Ordering Information

Part Number	Code	Operating Temperature	Package	MOQ	Description
FP5209KR-G1	AX	-25°C ~ 85°C	SOT23-5L	3000EA	Tape & Reel

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}		0		5.5	V
EN,FB Voltage			0		5.5	V
Power Dissipation	P_D	SOT23-5L @ $T_A=25^{\circ}\text{C}$			455	mW
Thermal Resistance (Note1)	θ_{JA}	SOT23-5L			+220	$^{\circ}\text{C} / \text{W}$
Junction Temperature	T_J				+150	$^{\circ}\text{C}$
Operating Temperature	T_{OP}		-25		+85	$^{\circ}\text{C}$
Storage Temperature	T_{ST}		-65		+150	$^{\circ}\text{C}$
Lead Temperature		(soldering, 10 sec)			+260	$^{\circ}\text{C}$

IR Re-flow Soldering Curve



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Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V _{IN}		2.4		5.5	V
Operating Temperature Range	T _A	Ambient Temperature	-25		+85	°C

DC Electrical Characteristics (V_{CC}=3.3V, T_A=25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
System Supply Input						
Input Supply Range	V _{CC}		2.4		5.5	V
Operating Start Voltage	V _{ST}				1.1	V
Under Voltage Lockout	V _{UVLO}			2.1		V
UVLO Hysteresis				0.1		V
Quiescent Current	I _{CC}	FB=1.0V, No switch		70		μA
Shutdown Current	I _{CC}	V _{EN} =GND		0.1		μA
Oscillator						
Operation Frequency	f _{OSC}	V _{FB} =0.6V		550		kHz
PFM Switching Duty Ratio	%			15		%
Maximum Duty Ratio	%			90		%
Soft-Start Time	t _{SS}			7		ms
Reference Voltage						
Feedback Voltage	V _{REF}		0.588	0.6	0.612	V
Enable Control						
Enable Voltage	V _{EN}		0.96			V
Shutdown Voltage	V _{EN}				0.6	V
External Transistor Connection current						
EXT Pin Output Current	I _{EXTH}			-105		mA
EXT Pin Output Current	I _{EXTL}			130		mA

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Function Description

Operation

The FP5209 is a voltage mode boost controller. The switching is a fixed frequency 550kHz and operates with pulse width modulation (PWM). An internal resistive divider provides 0.6V reference for the error amplifier. The FP5209 changes to PFM mode when output is light load. It can increase efficiency, but PFM mode also increases output voltage ripple.

Soft Start Function

Soft start circuitry is integrated into FP5209 to avoid inrush current during power on. After the IC is enabled, the output of error amplifier is clamped by the internal soft-start function, which causes PWM pulse width increasing slowly and thus reducing input surge current.

Shutdown Function

Drive Enable pin to ground to shut down the FP5209. Shutdown mode forces to turn off all internal circuitry, and reduces the VIN supply current to 0.1 μ A (typ). The Enable pin rising threshold is 0.96V (typ). Before any operation begins, the voltage at Enable pin must exceed 0.96V (typ).

Application Information

Inductor Selection

Inductance value is decided based on different condition. 3.3uH to 4.7uH inductance value is recommended for general application circuit. There are three important inductor specifications, DC resistance, saturation current and core loss. Low DC resistance has better power efficiency.

Capacitor Selection

The output capacitor is required to maintain the DC voltage. Low ESR capacitors are preferred to reduce the output voltage ripple. Ceramic capacitor of X5R and X7R are recommended, which have low equivalent series resistance (ESR) and wider operation temperature range.

Diode Selection

Schottky diodes with fast recovery times and low forward voltages are recommended. Ensure the diode average and peak current rating exceed the average output current and peak inductor current. In addition, the diode's reverse breakdown voltage must exceed the output voltage.

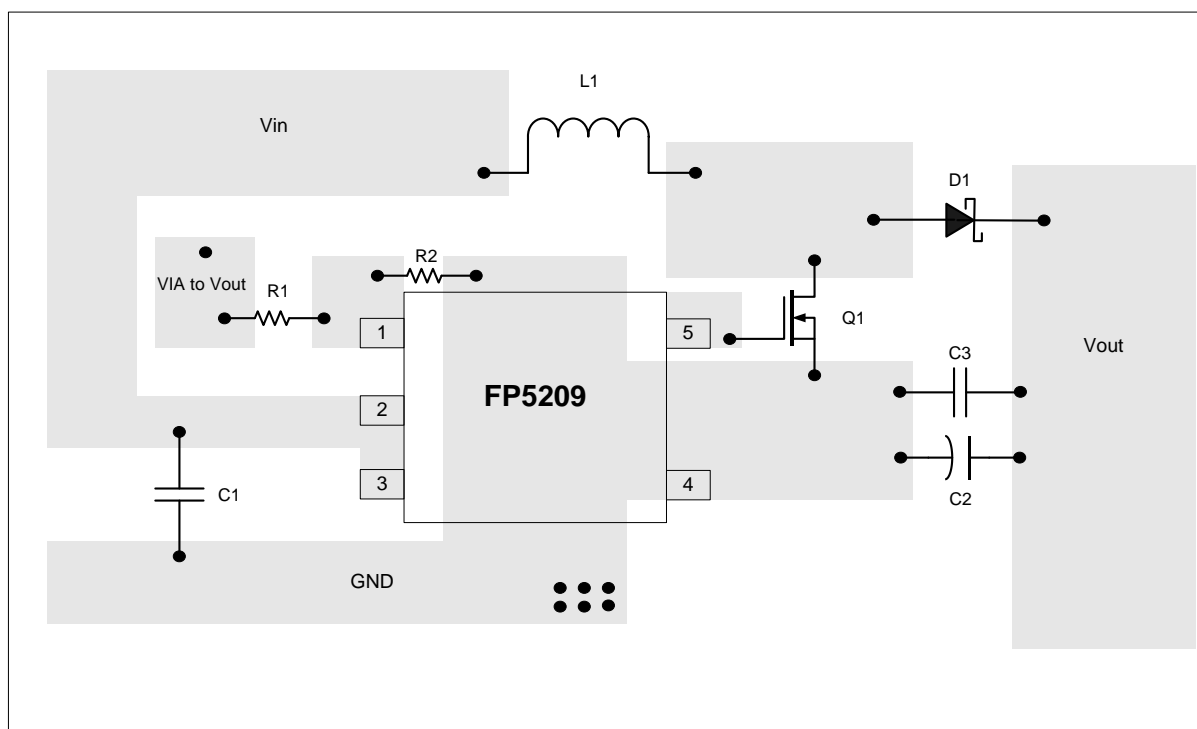
Output Voltage Programming

The output voltage is set by a resistive voltage divider from the output voltage to FB. The output voltage is:

$$V_{OUT} = 0.6V \left(1 + \frac{R1}{R2} \right)$$

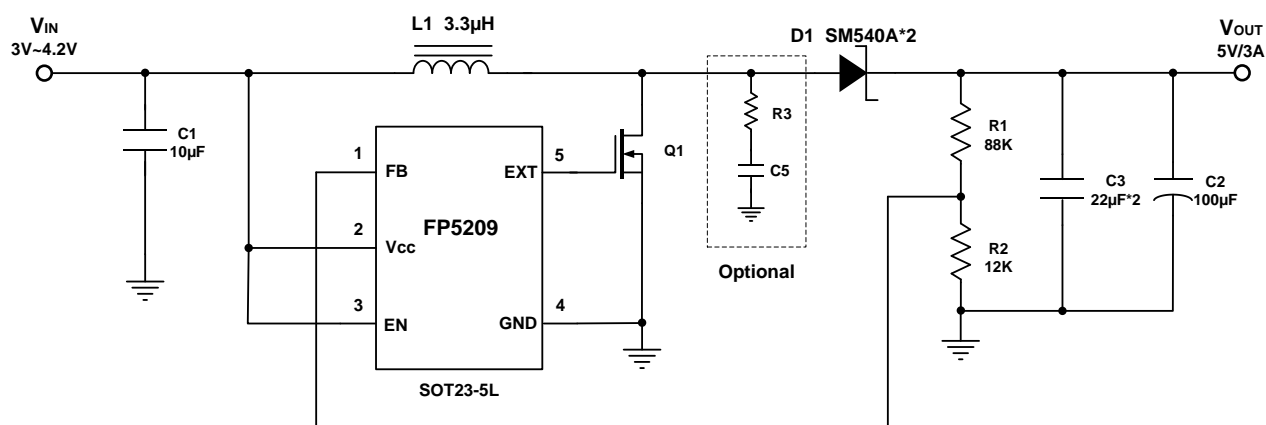
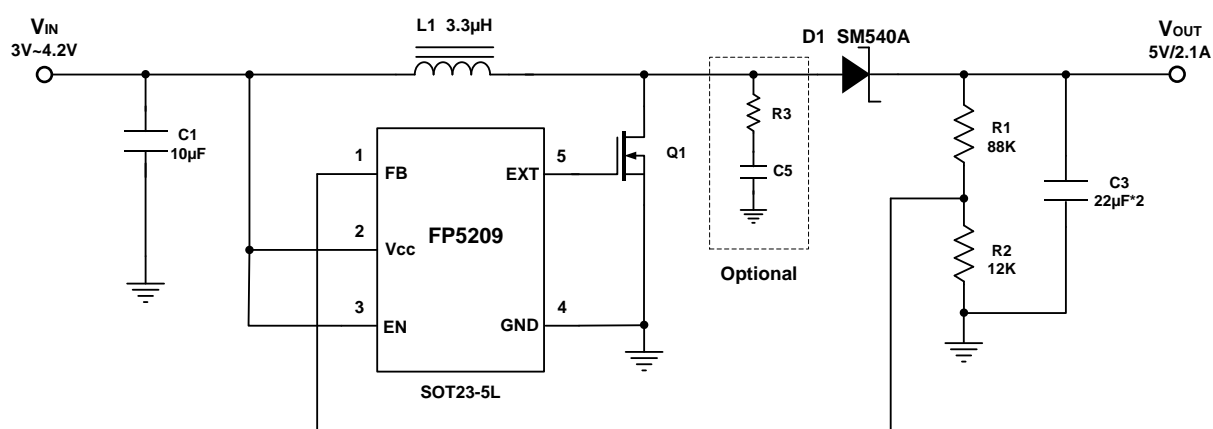
Layout Considerations

1. The power traces, consisting of the GND trace, the MOS drain trace and the V_{CC} trace should be kept short, direct and wide.
2. Layout switching node MOS drain, inductor and diode connection traces wide and short to reduce EMI.
3. Place C_{IN} nearby V_{CC} pin as closely as possible to maintain input voltage steady and filter out the pulsing input current.
4. The resistive divider R1 and R2 must be connected to FB pin directly and as closely as possible.
5. FB is a sensitive node. Please keep it away from switching node, MOS drain.
6. The GND of the IC, C_{IN} and C_{OUT} should be connected close together and directly to a ground plane.
7. The output capacitor C2 and C3 should be connected close and together directly to the source of MOS.



Suggested Layout

Application Information

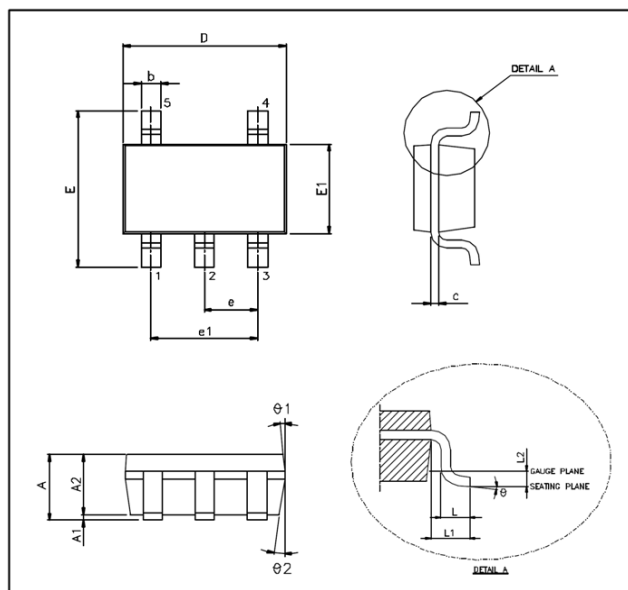


Note:

1. $C1$ and $C3$ choose ceramic capacitor of X5R or X7R.
2. $R3$ and $C5$ are added for reducing EMI (Electromagnetic Interference).

Package Outline

SOT23-5L



Unit: mm

Symbols	Min. (mm)	Max.(mm)
A	1.050	1.350
A1	0.050	0.150
A2	1.000	1.200
b	0.250	0.500
c	0.080	0.200
D	2.700	3.000
E	2.600	3.000
E1	1.500	1.700
e	0.950 BSC	
e1	1.900 BSC	
L	0.300	0.550
L1	0.600 REF	
L2	0.250 BSC	
θ°	0°	10°
θ1°	3°	7°
θ2°	6°	10°

Note:

- Package dimensions are in compliance with JEDEC outline: MO-178 AA.
- Dimension “D” does not include molding flash, protrusions or gate burrs.
- Dimension “E1” does not include inter-lead flash or protrusions.

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