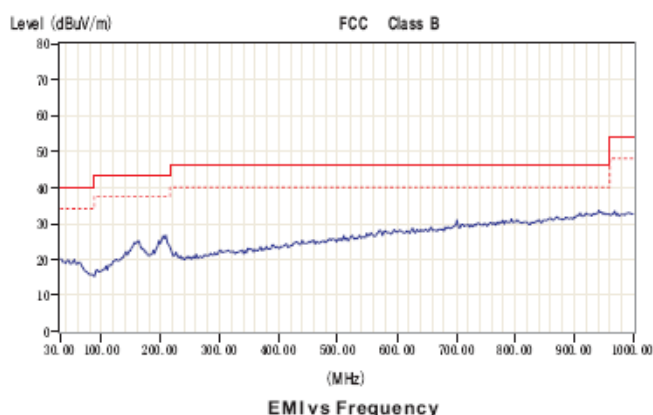


Ultra Low EMI, 3W Filterless Mono Class-D Audio Power Amplifier, ME5103

General Description

ME5103 is a 3W mono filterless class-D amplifier with high PSRR and differential input that eliminate noise and RF rectification. The filterless architecture requires no external output filter, fewer external components, less PCB area and lower system costs, and simplifies application design. It features short circuit protection and thermal shutdown.



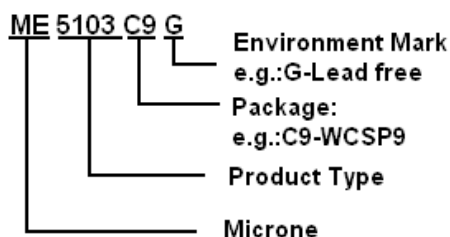
Features

- Ultra Low EMI, -20dB Better Than FCC Class-B@ 300MHz
- High Efficiency up to 92% @ 1W with an 8Ω Speaker
- Shutdown Current < 1uA
- 3W @ 10% THD Output with a 4Ω Load at 5V Supply
- Demanding few external components
- Supply voltage from 2.5V to 5.5V
- Short circuit protection, Thermal shutdown, UVLO
- Available in Space Saving Packages:
1.45mmX1.45mm WCSP9
- Pb-Free Package

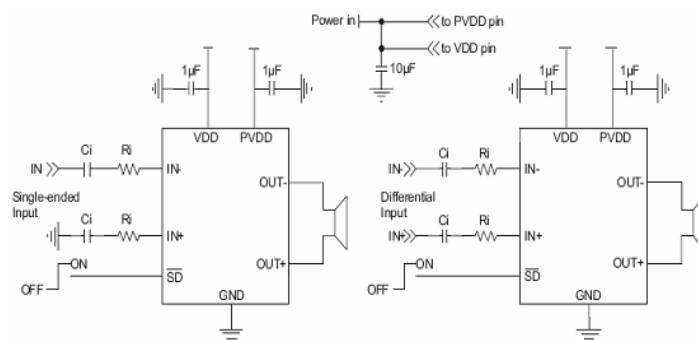
Typical Application

- Cellular Phones/Smart Phones MP4/MP3
- MP4/MP3 GPS
- Digital Photo Frame
- Electronic Dictionary
- Portable Game Machines

Selection Guide

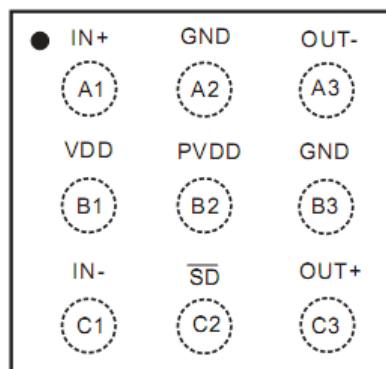


Typical Application Circuit



Pin Configuration

9 Ball WCSP
Top View



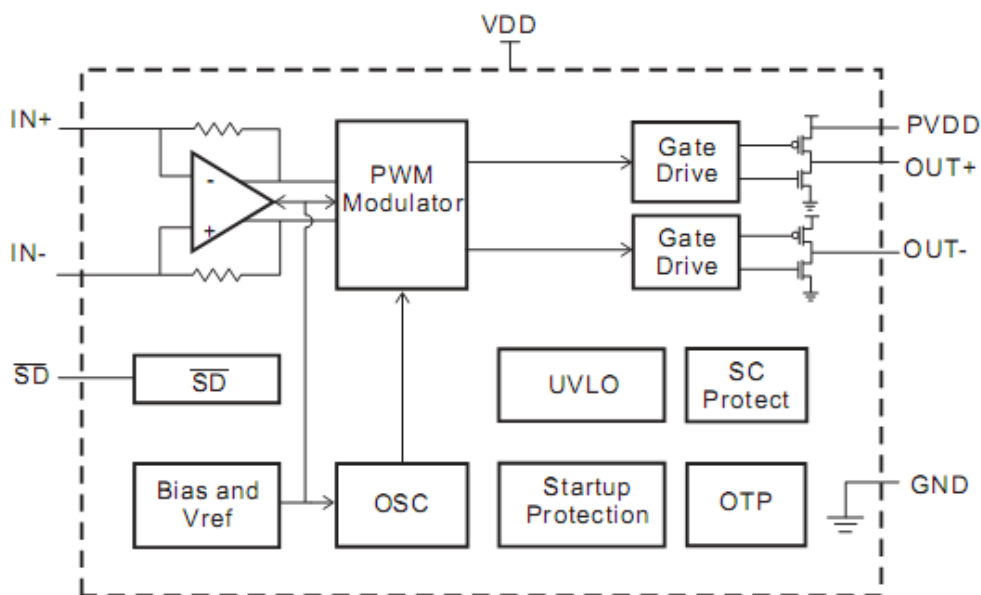
Pin Assignment

Pin Number	Pin Name	Description
1	OUT-	Positive output
2	PVDD	Power supply
3	VDD	Analog power supply
4	IN-	Negative differential input
5	IN+	Positive differential input
6	\overline{SD}	shutdown terminal, active low
7	GND	Ground
8	OUT+	Negative output

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Units
Supply Voltage	V_{DD}	6.5	V
Input Voltage	V_{in}	-0.3 to $V_{DD}+0.3$	V
Operating Temperature Range	T_{OPR}	-40~+85	°C
Storage Temperature Range	T_{STG}	-65~+150	°C
Maximum Junction Temperature	T_{MJ}	150	°C
Soldering Temperature	T_{SD}	250,10	°C,sec

Block Diagram



Electrical Characteristics

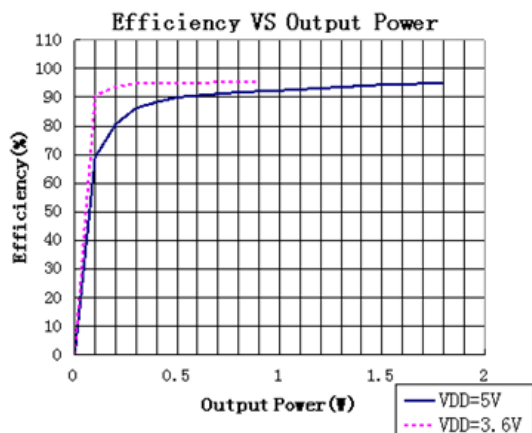
$T_A=25^{\circ}\text{C}$, $V_{DD}=5\text{V}$, Gain=2.3V/V, $R_L=L(33\mu\text{H})+R+L(33\mu\text{H})$, unless otherwise noted.

Symbol	Parameter	Test Conditions		MIM	TYP	MAX	UNIT
V_{DD}	Supply Voltage			2.5		5.5	V
P_O	Output Power	THD+N=10%,f=1kHz,R=4 Ω	$V_{DD}=5.0\text{V}$		3.3		W
			$V_{DD}=3.6\text{V}$		1.69		
			$V_{DD}=3.2\text{V}$		1.33		
		THD+N=1%,f=1kHz,R=4 Ω	$V_{DD}=5.0\text{V}$		2.66		W
			$V_{DD}=3.6\text{V}$		1.35		
			$V_{DD}=3.2\text{V}$		1.06		
		THD+N=10%,f=1kHz,R=8 Ω	$V_{DD}=5.0\text{V}$		1.83		W
			$V_{DD}=3.6\text{V}$		0.94		
			$V_{DD}=3.2\text{V}$		0.74		
		THD+N=1%,f=1kHz,R=8 Ω	$V_{DD}=5.0\text{V}$		1.45		
			$V_{DD}=3.6\text{V}$		0.75		
			$V_{DD}=3.2\text{V}$		0.59		
THD+N	Total Harmonic Distortion Plus Noise	$V_{DD}=5.0\text{V},P_O=1\text{W},R=8\Omega$	f=1kHz		0.79		%
		$V_{DD}=3.6\text{V},P_O=0.1\text{W},R=8\Omega$			0.56		
		$V_{DD}=3.2\text{V},P_O=0.1\text{W},R=8\Omega$			0.51		

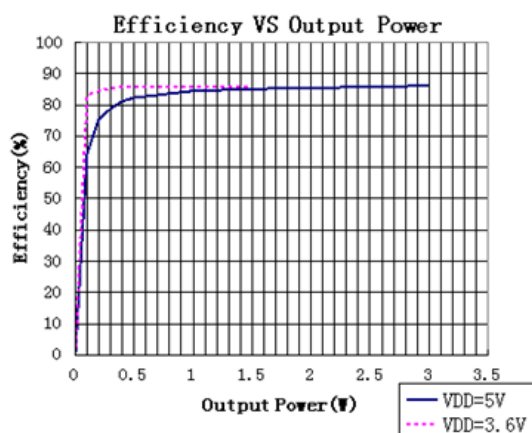
		V _{DD} =5.0V, P _O =0.5W, R=4Ω	f=1kHz		0.82		%
		V _{DD} =3.6V, P _O =0.2W, R=4Ω			0.56		
		V _{DD} =3.2V, P _O =0.1W, R=4Ω			0.51		
PSRR	Power Supply Ripple Rejection	V _{DD} =3.6V, Inputs ac-grounded with C=1μF	f=217Hz		-63	-55	dB
			f=1kHz		-62	-55	
			f=10kHz		-52	-40	
Dyn	Dynamic Range	V _{DD} =5V, THD=1%, R=8Ω	f=1kHz	52.6	90		
V _n	Output Noise	Inputs ac-grounded	No A-weighting		100		μV
			A-weighting		65		
CMRR	Common Mode Rejection Ratio	V _{IC} =100mV _{pp} , f=1kHz			56		dB
η	Efficiency	R _L =8Ω, THD=10%	f=1kHz		95		%
		R _L =4Ω, THD=10%			86		
I _Q	Quiescent Current	V _{DD} =5.0V	R=8Ω		3	8	mA
		V _{DD} =3.6V			1.5	5	
		V _{DD} =3.0V			1	1.5	
I _{SD}	Shutdown Current	V _{DD} =3.0V to 5V	V _{SD} =0.3V		0.1	2	μA
R _{dson}	Static Drain-to-source On-state Resistor	CSP package, high side P MOS plus Low side N MOS, I=500mA	V _{DD} =5.0V		266		mΩ
			V _{DD} =3.6V		245		
			V _{DD} =3.0V		240		
R _i	Input Resistance				150		kΩ
f _{sw}	Switching Frequency	V _{DD} =3V to 5V		200	250	300	kHz
G _v	Closed-loop Gain	V _{DD} =3V to 5V			350kΩ/R _i		V/V
V _{OS}	Output Offset Voltage	Input ac-ground, V _{DD} =5V			13	50	mV
V _{IH}	Enable Input High Voltage	V _{DD} =5V		1.5			V
V _{IL}	Enable Input Low Voltage	V _{DD} =5V				0.5	

Type Characteristics ($T_A=25^{\circ}\text{C}$, $V_{DD}=5\text{V}$, $f=1\text{kHz}$, $\text{Gain}=2.3\text{V/V}$, unless otherwise noted.)

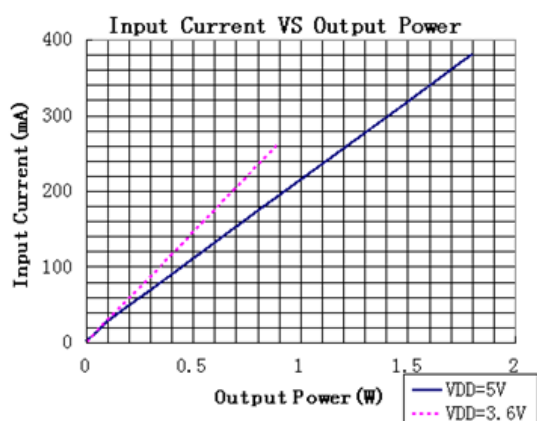
(1) Efficiency VS Output Power($R_L=8\Omega$)



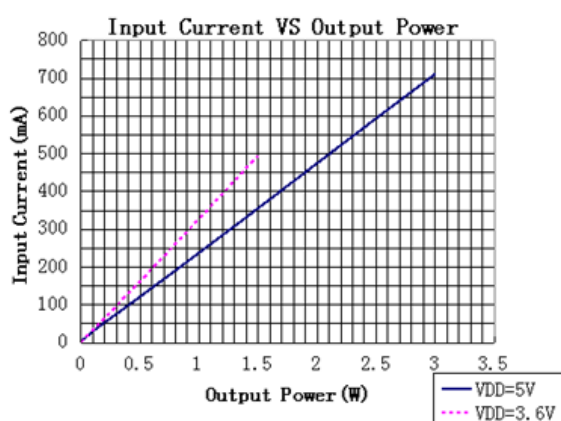
(2) Efficiency VS Output Power($R_L=4\Omega$)



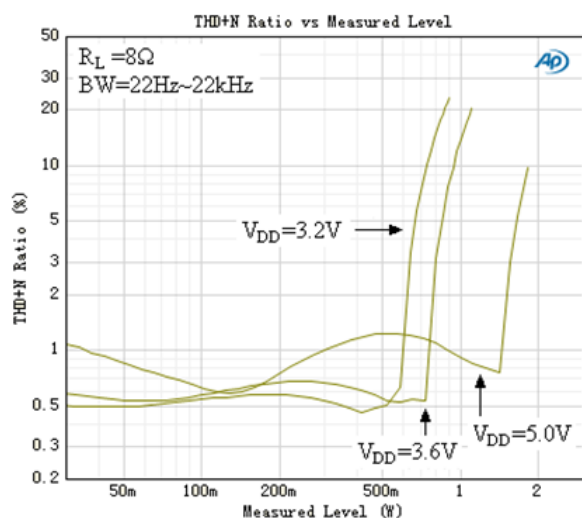
(3) Input Current VS Output Power($R_L=8\Omega$)



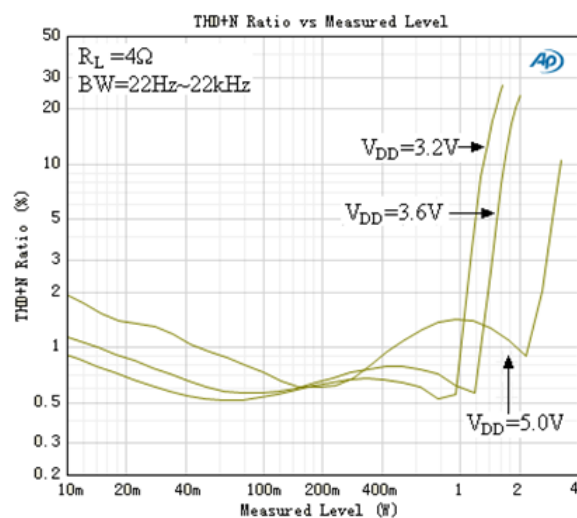
(4) Input Current VS Output Power($R_L=4\Omega$)



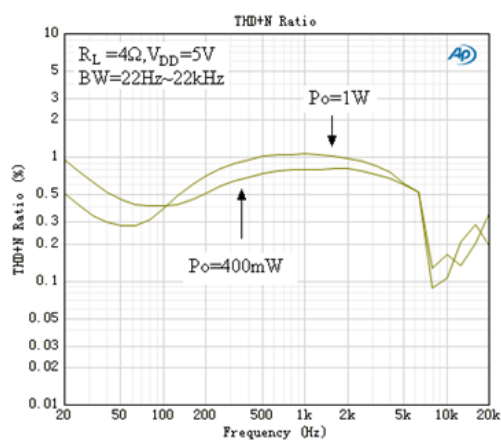
(5) THD+N VS Output Power($R_L=8\Omega$)



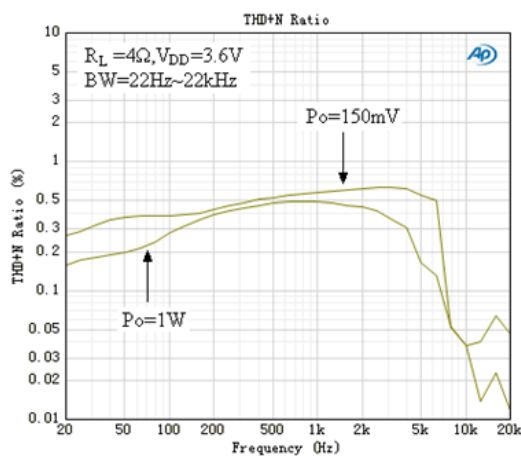
(6) THD+N VS Output Power ($R_L=4\Omega$)



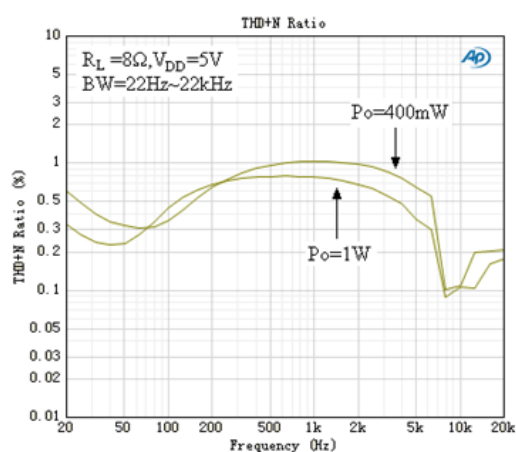
(7) THD+N VS Frequency ($R_L=4\Omega, V_{DD}=5V$)



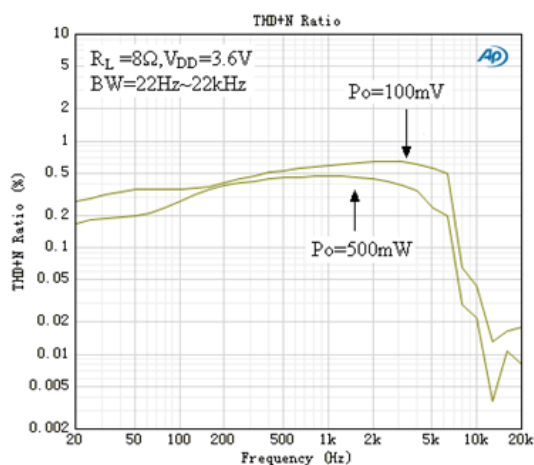
(8) THD+N VS Frequency ($R_L=4\Omega, V_{DD}=3.6V$)



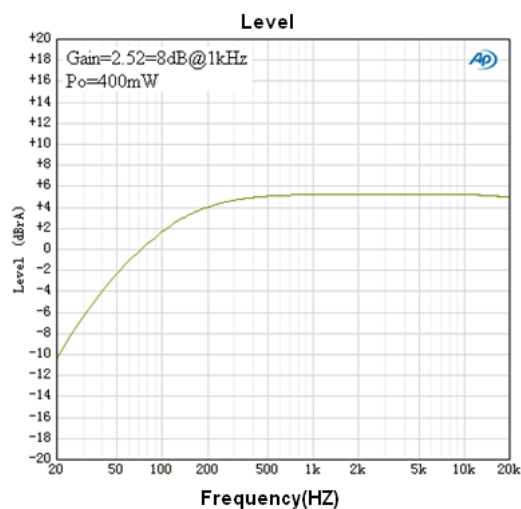
(9) THD+N VS Frequency ($R_L=8\Omega, V_{DD}=5V$)



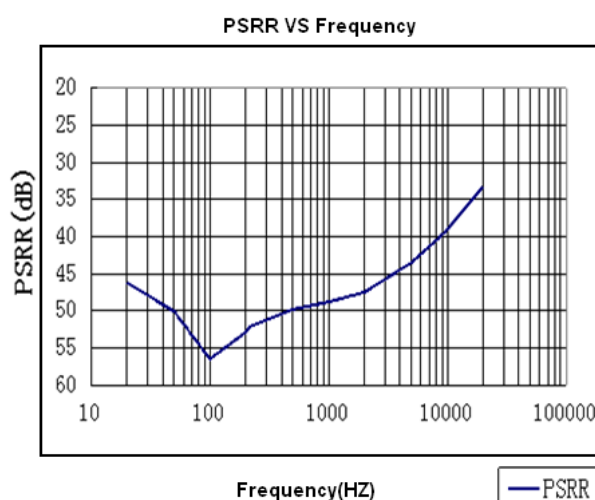
(10) THD+N VS Frequency ($R_L=8\Omega, V_{DD}=3.6V$)



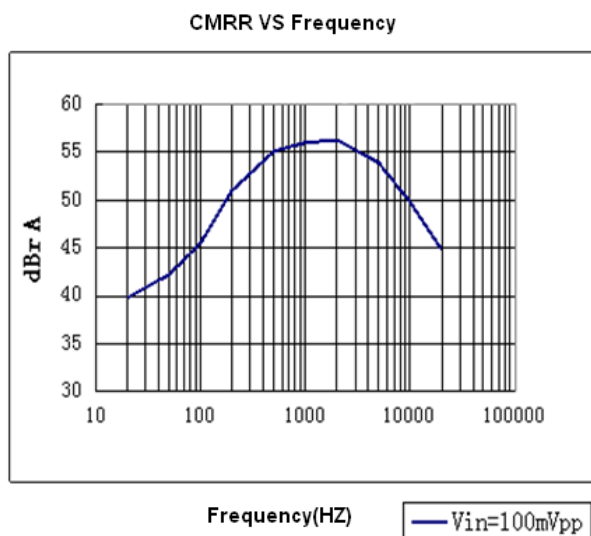
(11) Frequency Response



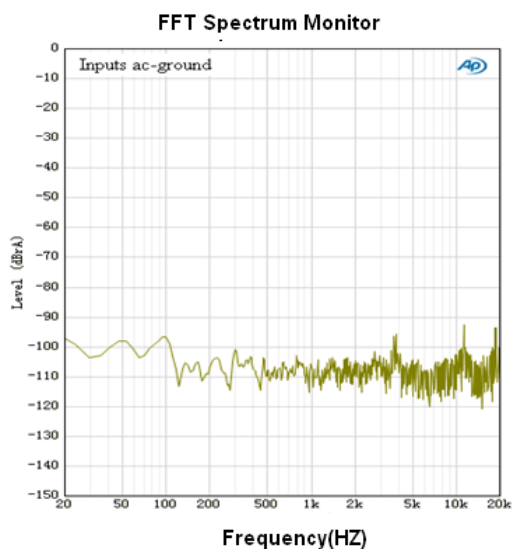
(12) PSRR VS Frequency



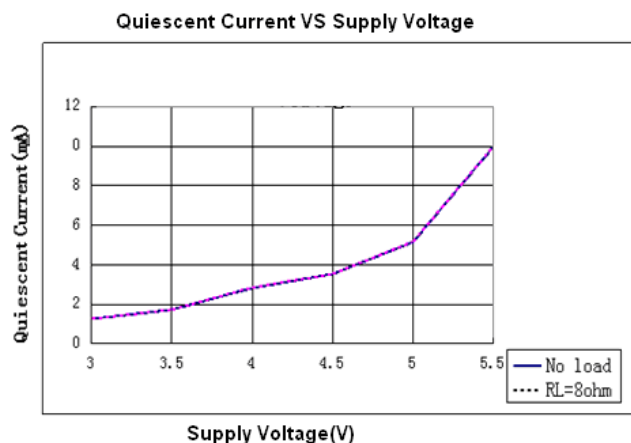
(13) CMRR VS Frequency



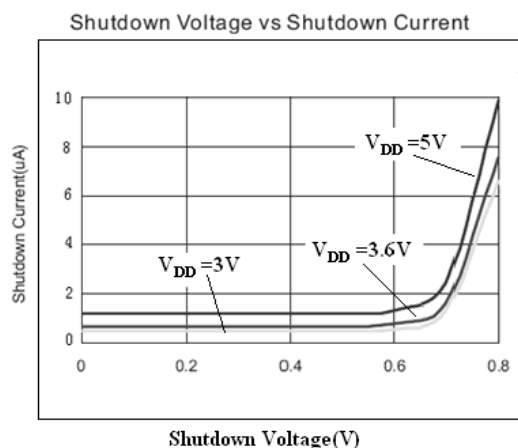
(14) Noise FFT(inputs ac-ground)



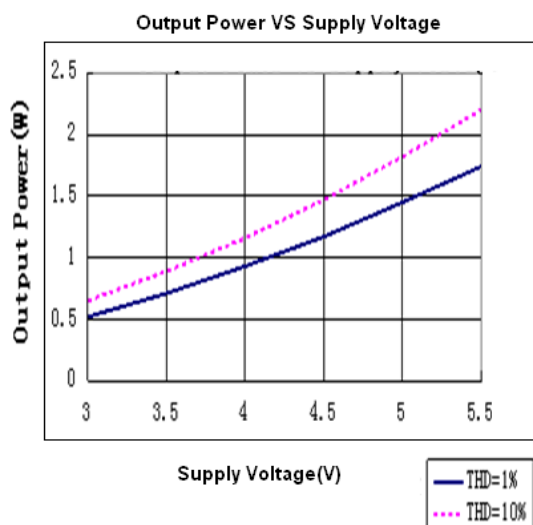
(15) Quiescent Current VS Power Supply Voltage



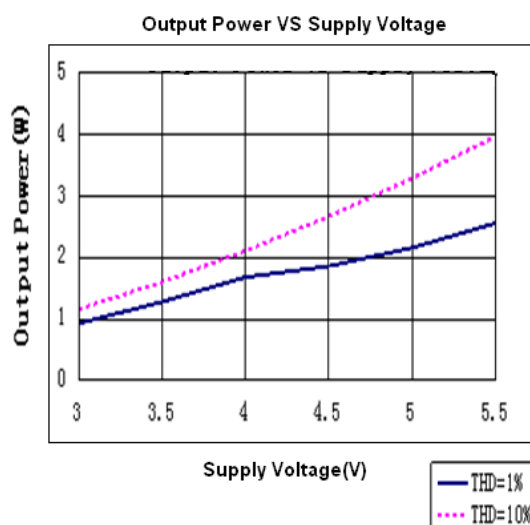
(16) Shutdown Voltage VS Shutdown Current



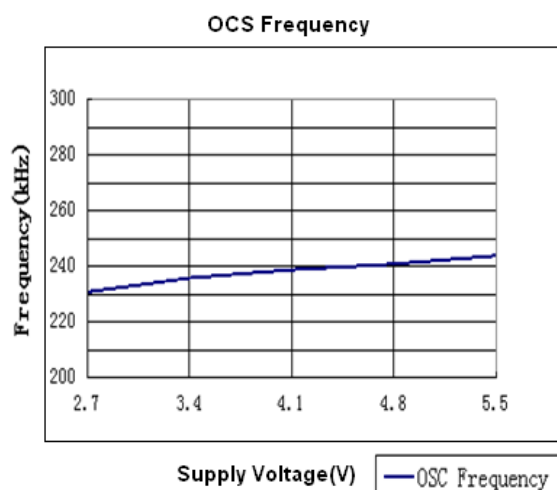
(17) Output Power VS Supply Voltage($R_L=8\Omega$)



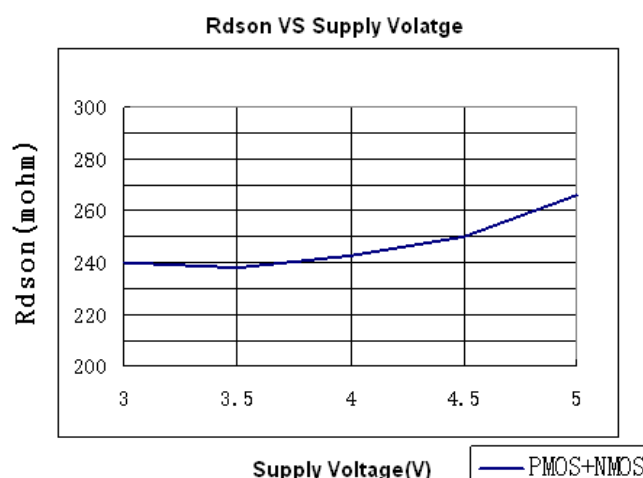
(18) Output Power VS Supply Voltage($R_L=4\Omega$)



(19) OSC Frequency



(20) Rdson VS Supply Voltage



Application Guideline:

1. Input resistors (Ri):

The input resistors (Ri) set the gain of the amplifier according to Equation:

$$\text{Gain} = \frac{350\text{k}\Omega}{R_i}$$

Resistor matching is very important in fully differential amplifiers. It is recommended to use 1% tolerance and 1% matching resistors or better to keep the performance optimized. Place the input resistors very close to the IC to limit noise injection on the high impedance nodes. Lower gain allows the IC to operate at its best, and making the inputs less susceptible to noise.

2. Input capacitor (Ci):

Ci and the minimum input impedance Ri form a high-pass filter with the corner frequency determined in the follow equation:

$$f_c = \frac{1}{2\pi R_i C_i}$$

When input resistance variation is considered, the Ci is 7nF, so one would likely choose a value of 10nF. A further consideration for this capacitor is not to use a polarized capacitor but to use a low-leakage tantalum or ceramic capacitor.

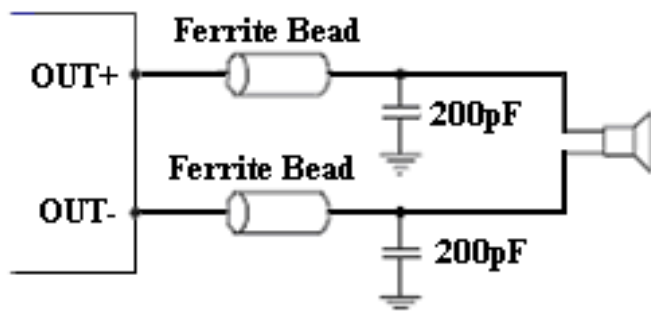
3. Decoupling Capacitor (Cs):

Power supply decoupling to ensure the output total harmonic distortion (THD) as low as possible and prevents the oscillations causing by long lead length between the amplifier and the speaker.

The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads: For higher frequency transients spikes, or digital hash on the line, a good low equivalent series-resistance (ESR) ceramic capacitor, typically 1uF, is placed as close as possible to the device each VDD and PVDD pin for the best operation. For filtering lower frequency noise signals, a large ceramic capacitor of 10uF or greater placed near the audio power amplifier is recommended.

4. How to reduce EMI

Most applications require a ferrite bead filter for EMI elimination shown at Figure. The ferrite filter reduces EMI around 1MHz and higher. When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.



5. Shutdown operation

In order to reduce power consumption while not in use, the IC contains shutdown circuitry that is used to turn off the amplifier's bias circuitry. This shutdown feature turns the amplifier off when logic low is placed on the pin, the IC supply current draw will be minimized in idle mode.

6. Under Voltage Lock-out (UVLO)

When the supply voltage drops to 2.3V or below, the IC goes into a state of shutdown, and the device comes out of its shutdown state and restore to normal function only when reset the power supply or \overline{SD} pin.

7. Short Circuit Protection (SCP)

The IC immediately goes into shutdown state to prevent the device from damage when output-to-output shorts or output-to-GND shorts occur. Once the short is removed, the device will be reactivated.

8. Over Temperature Protection (OTP)

Once the die temperature exceeds the set point (135°C , there is a 15°C tolerance on this trip point from device to device), the device will enter the shutdown state and the outputs are disabled to prevents the device from damage. This is not a latched fault. The thermal fault is cleared once the temperature of the die decreased by 30°C .

9. POP and Click Circuitry

The IC contains circuitry to minimize turn-on and turn-off transients or "click and pops", where turn-on refers to either power supply turn-on or device recover from shutdown mode.

PCB Layout Guideline:

1. Grounding

It is recommended to use plane grounding or separate grounds. Do not use one line connecting power GND and analog GND. Signal currents for the inputs, reference need to be returned to quiet ground. This ground only ties to the signal components and the GND pin. GND then ties to system ground.

2. Power supply line

VDD and PVDD need to be separately connected to the system power supply. It is recommended that all the trace could be routed as short and thick as possible.

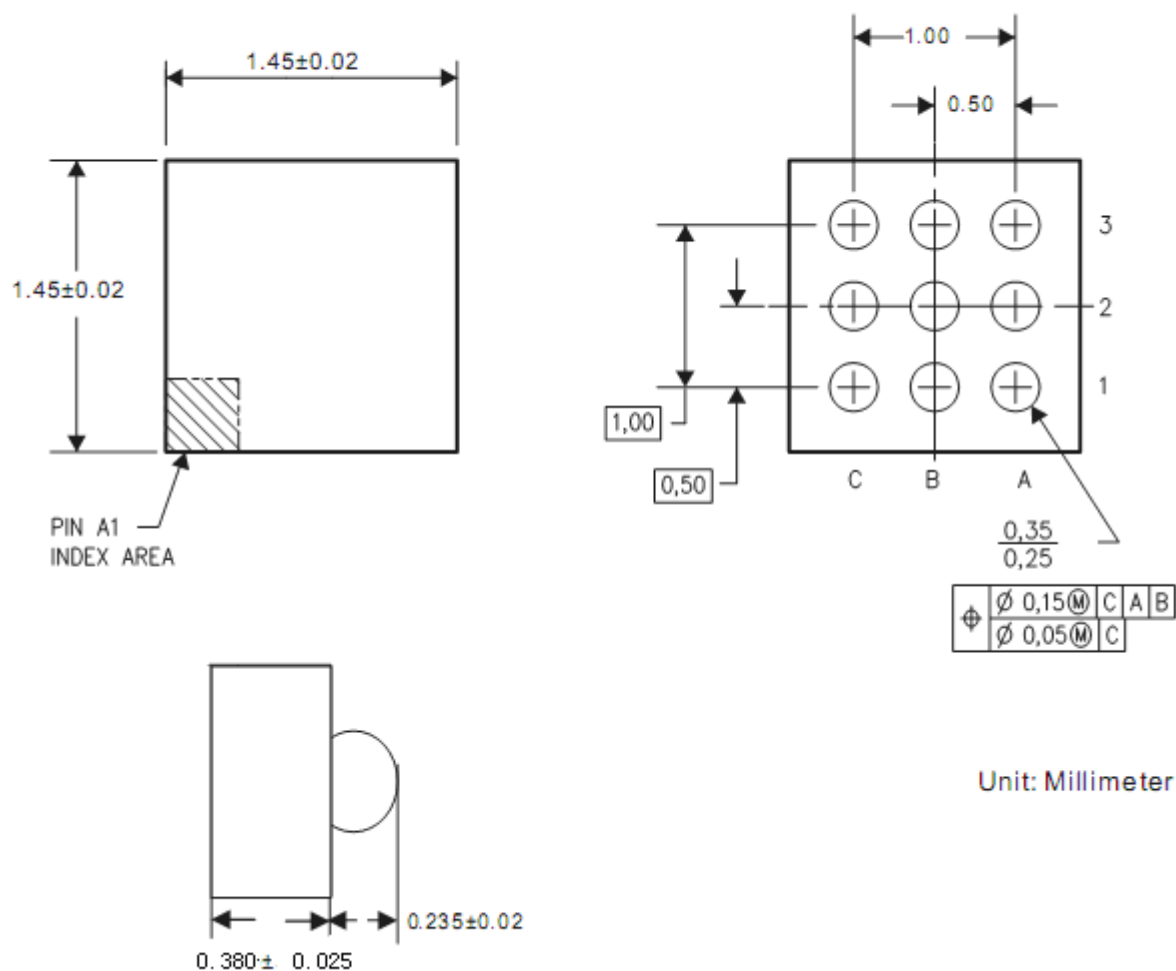
3. Components placement

Decoupling capacitors-As previously described, the high-frequency 1uF decoupling capacitors should be placed as close to the power supply terminals (VDD and PVDD) as possible. Large bulk power supply decoupling capacitors (10uF or greater) should be placed near the IC on the PVDD terminal.

Input resistors and capacitors need to be placed very close to input pins. Output filter-The ferrite EMI filter should be placed as close to the output terminals as possible for the best EMI performance, and the capacitors used in the filters should be grounded to system ground.

Packaging Information:

WCSP



Unit: Millimeter

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